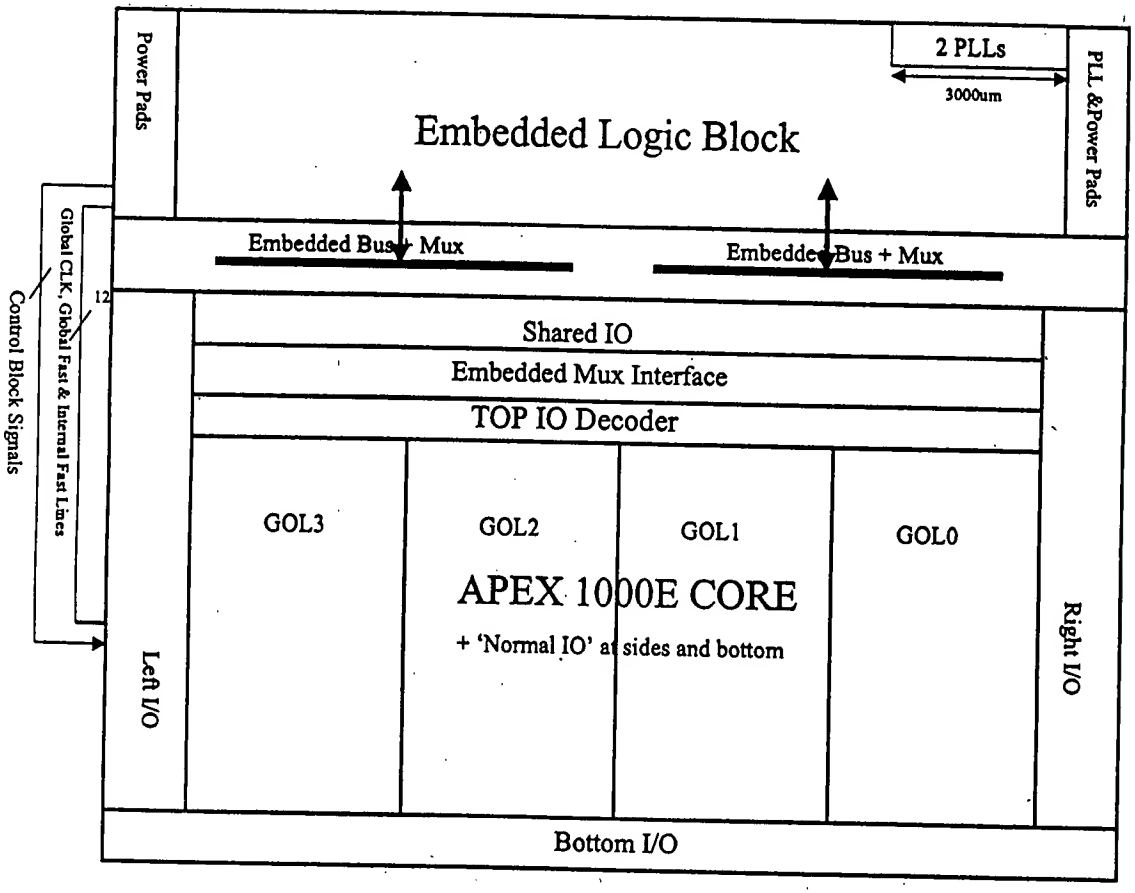


Top Level Floorplan

FIGURE 2

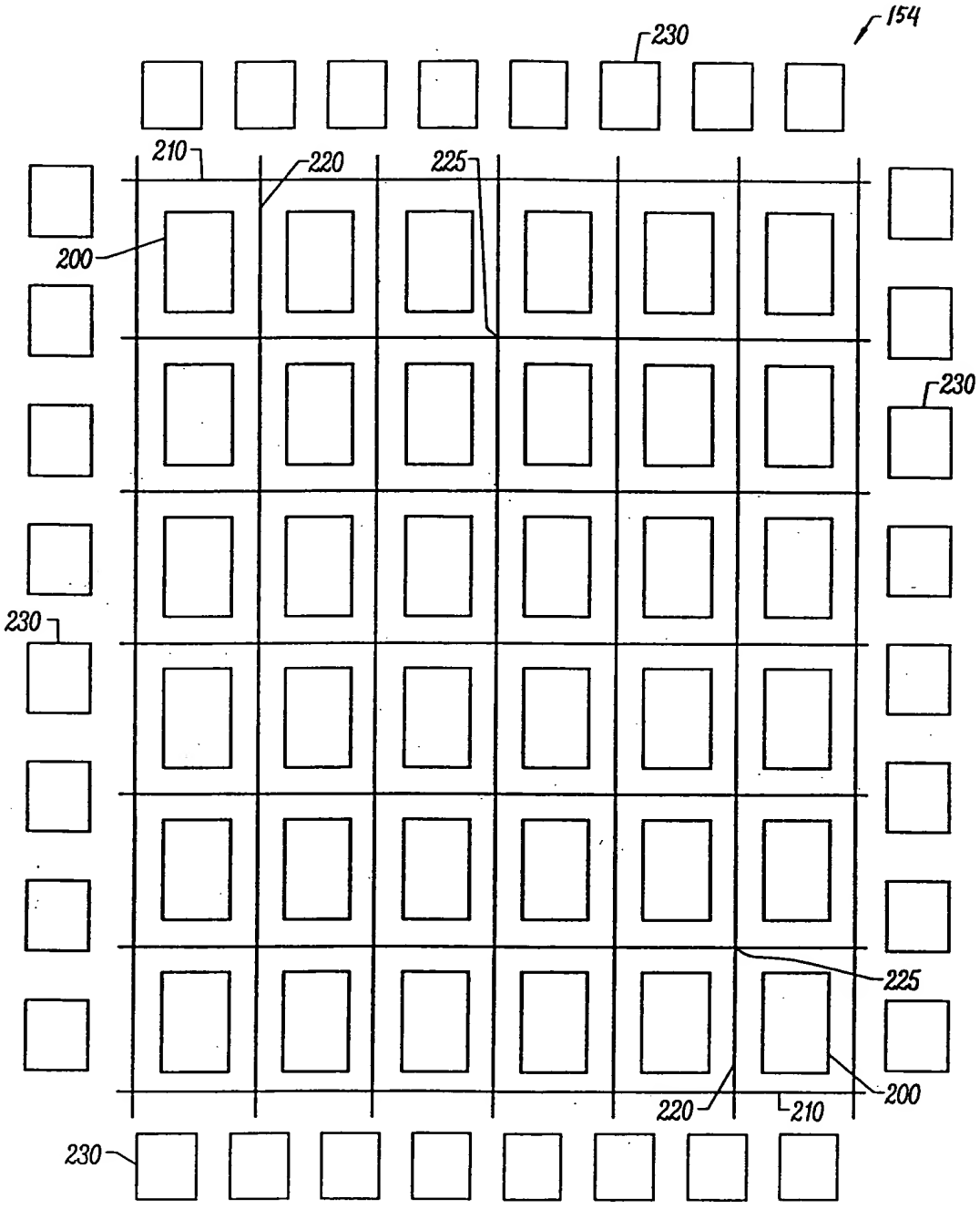


FIGURE 3

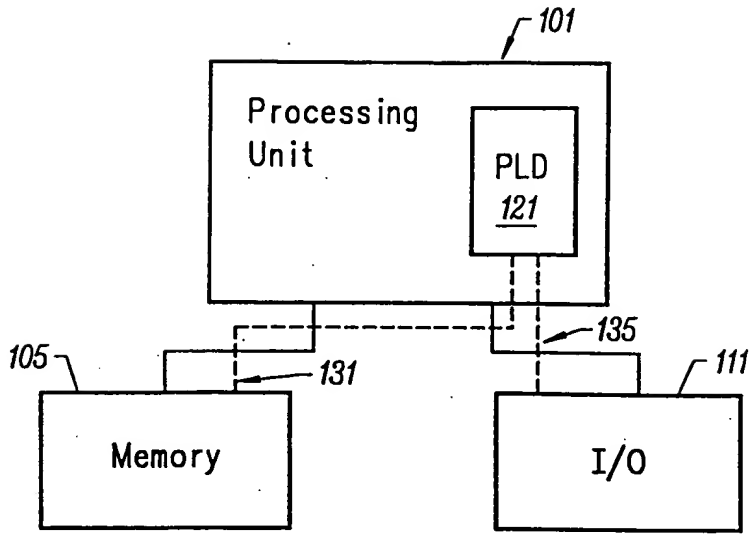


FIGURE 1

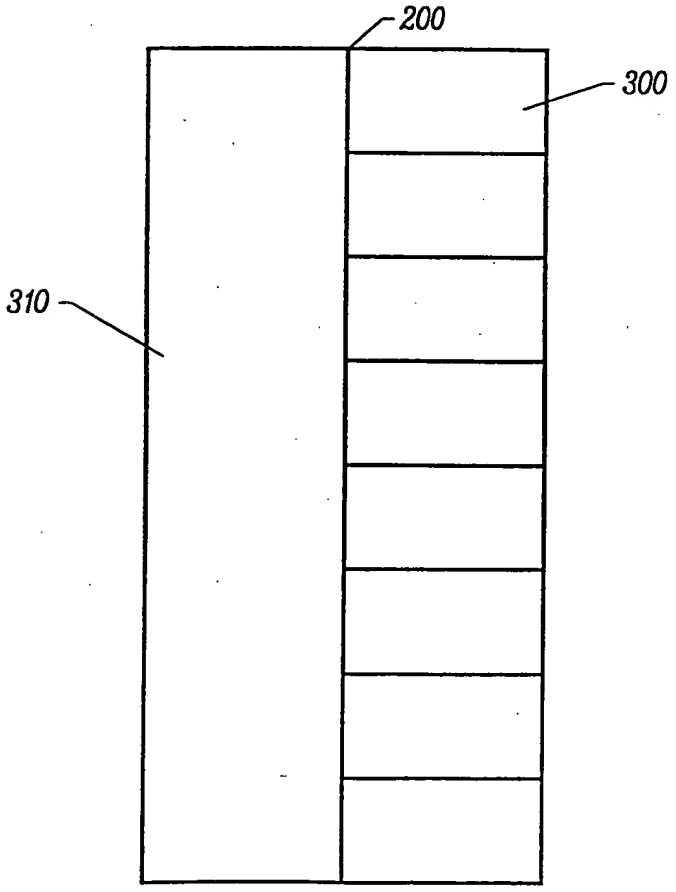


FIGURE 4

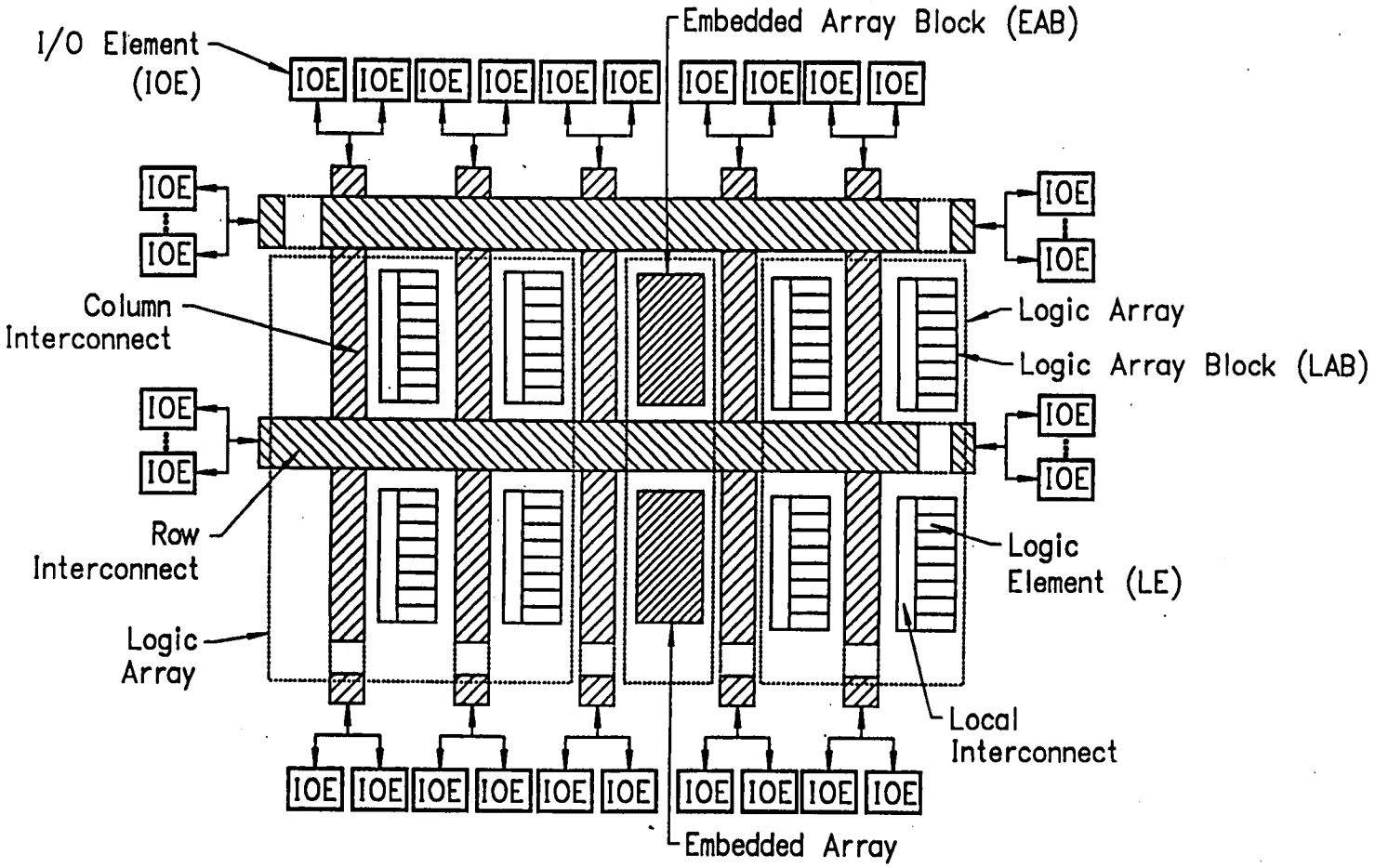

I/O Element
(IOE)
Embedded Array Block (EAB)
IOE
Column
Interconnect
Logic Array
Logic Array Block (LAB)
Row
Interconnect
Logic
Element (LE)
Logic
Array
Local
Interconnect
Embedded Array

FIGURE 5

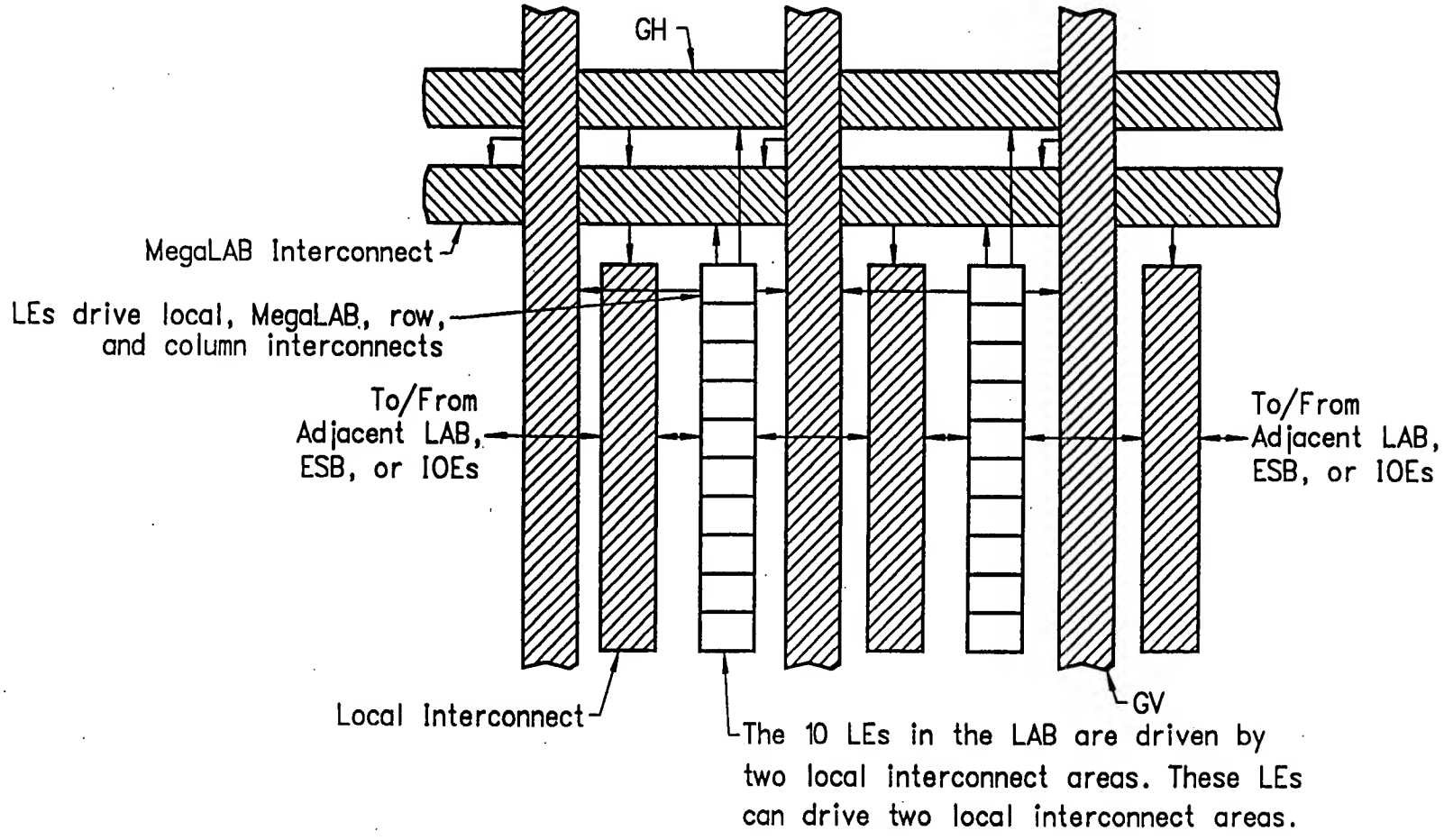

GH
MegaLAB Interconnect
LEs drive local, MegaLAB, row, and column interconnects
To/From Adjacent LAB, ESB, or IOEs
To/From Adjacent LAB, ESB, or IOEs
Local Interconnect
GV
The 10 LEs in the LAB are driven by two local interconnect areas. These LEs can drive two local interconnect areas.

FIGURE 6

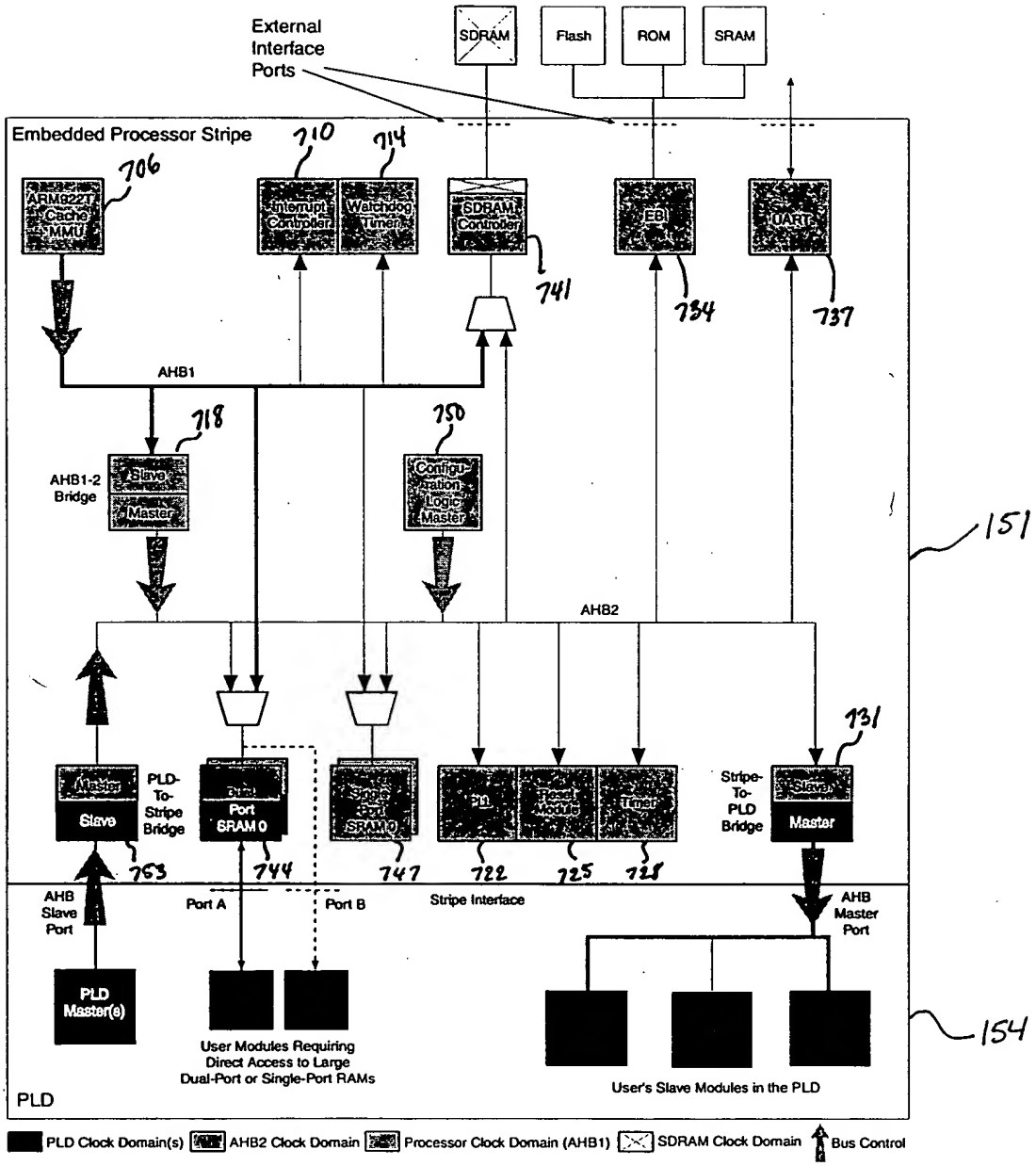


FIGURE 7

FIGURE 8

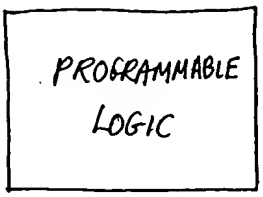


FIGURE 9

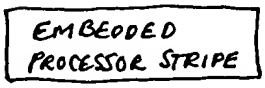


FIGURE 10

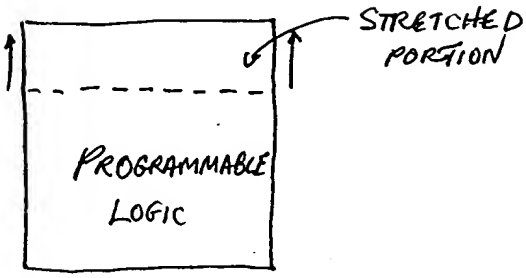
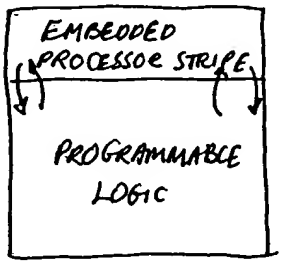


FIGURE 11



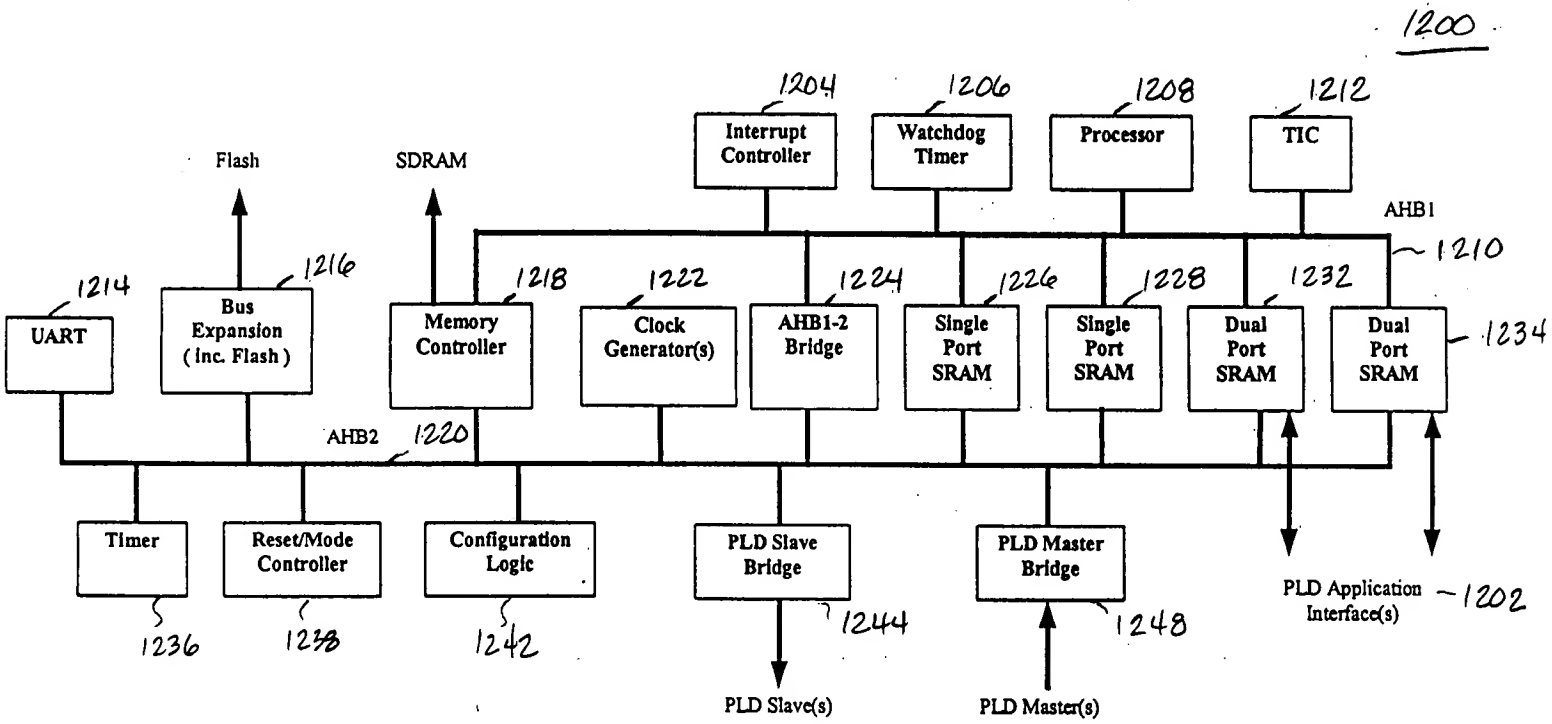
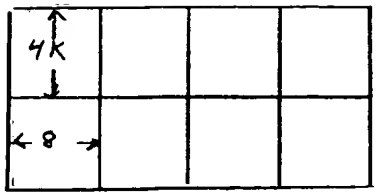

1200
1204
1206
1208
1212
Interrupt Controller
Watchdog Timer
Processor
TIC
Flash
SDRAM
AHB1
1210
1214
1216
1218
1222
1224
1226
1228
1232
1234
UART
Bus Expansion (Inc. Flash)
Memory Controller
Clock Generator(s)
AHB1-2 Bridge
Single Port SRAM
Single Port SRAM
Dual Port SRAM
Dual Port SRAM
AHB2
1220
Timer
Reset/Mode Controller
Configuration Logic
PLD Slave Bridge
PLD Master Bridge
PLD Application Interface(s)
1202
1236
1238
1242
1244
1248
PLD Slave(s)
PLD Master(s)

FIGURE 12

32

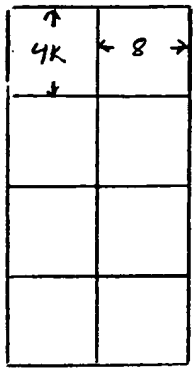


8K

8K x 32

FIGURE 13A

16

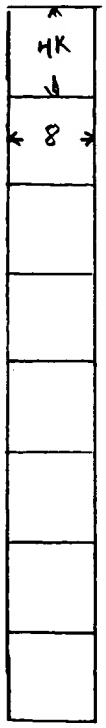


16K

16K x 16

FIGURE 13B

8



32K

32K x 8

FIGURE 13C

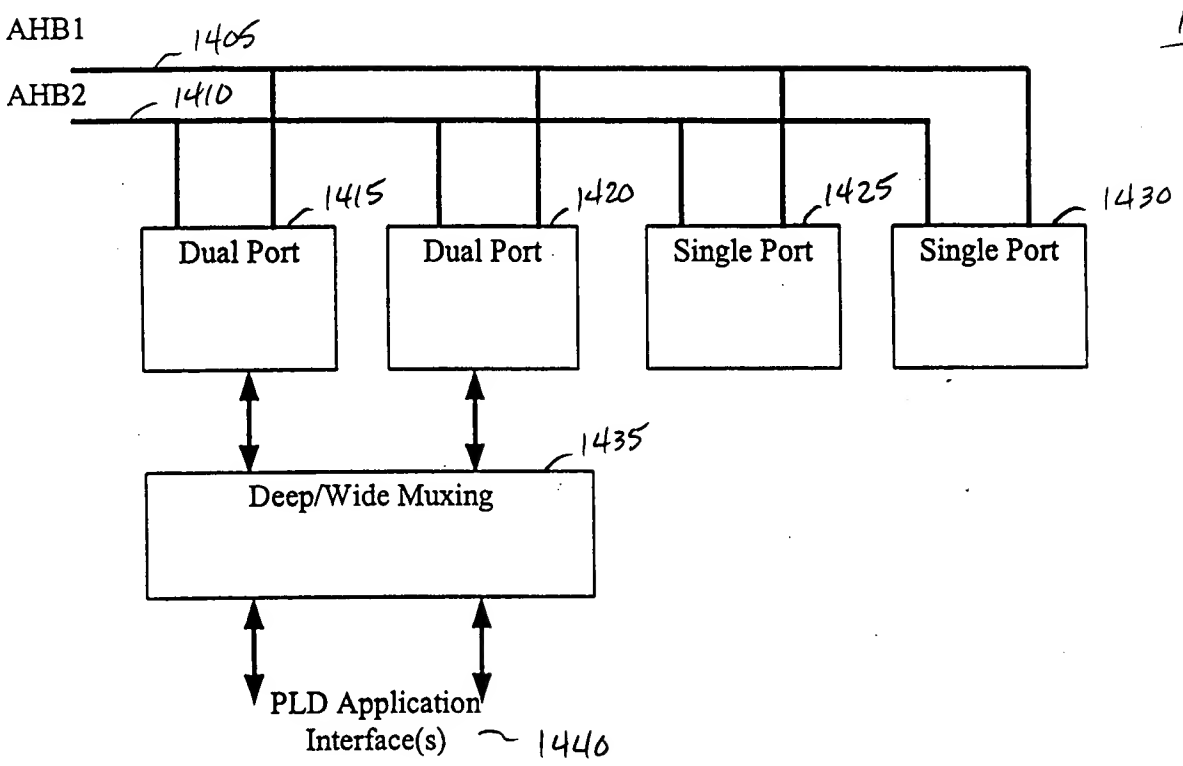


FIGURE 14

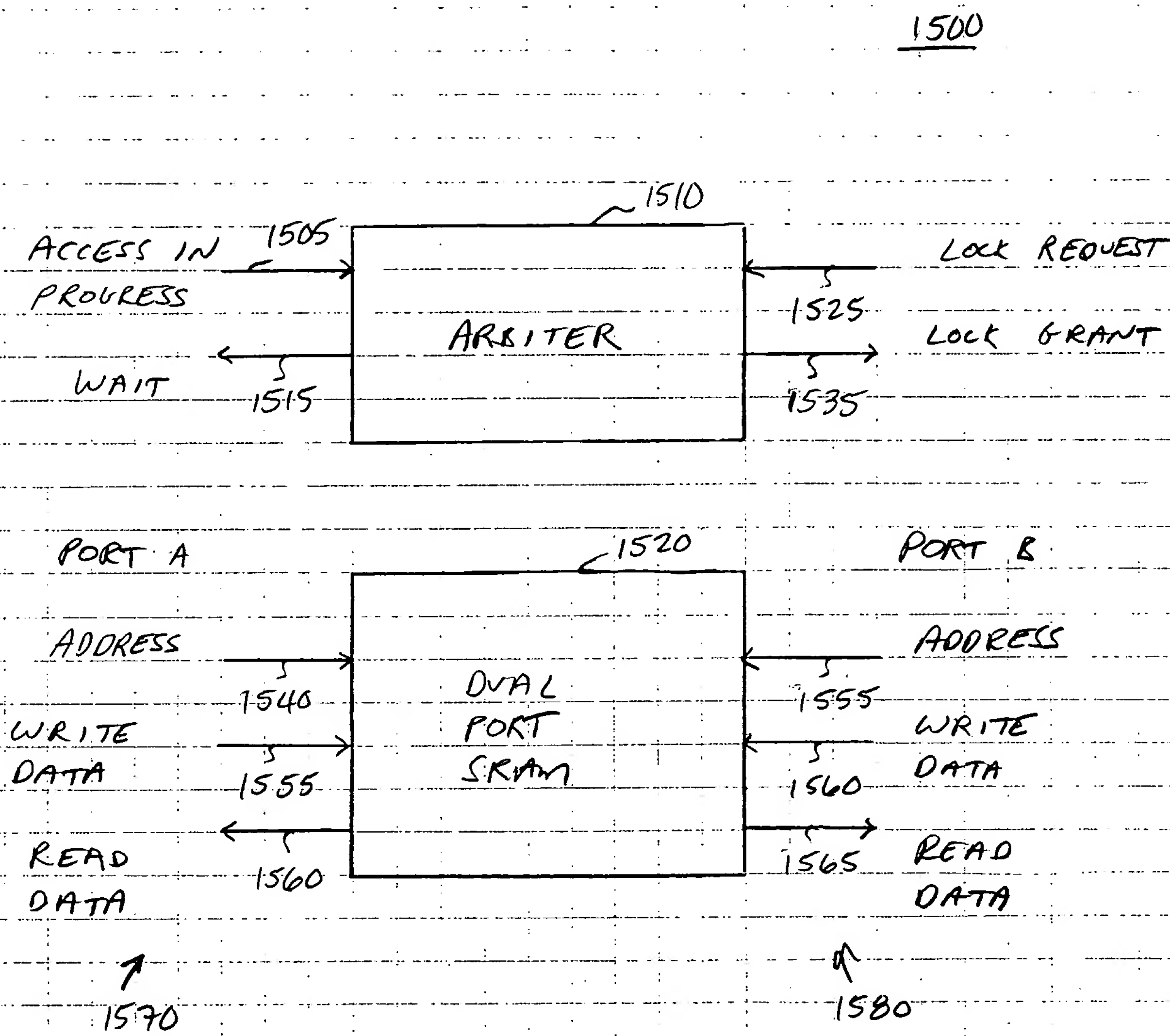

1500
1510
ACCESS IN PROGRESS
1505
WAIT
1515
ARBITER
LOCK REQUEST
1525
LOCK GRANT
1535
PORT A
1520
PORT B
ADDRESS
1540
WRITE DATA
1555
READ DATA
1560
DUAL PORT SRAM
ADDRESS
1555
WRITE DATA
1560
READ DATA
1565
1570
1580

Figure 15

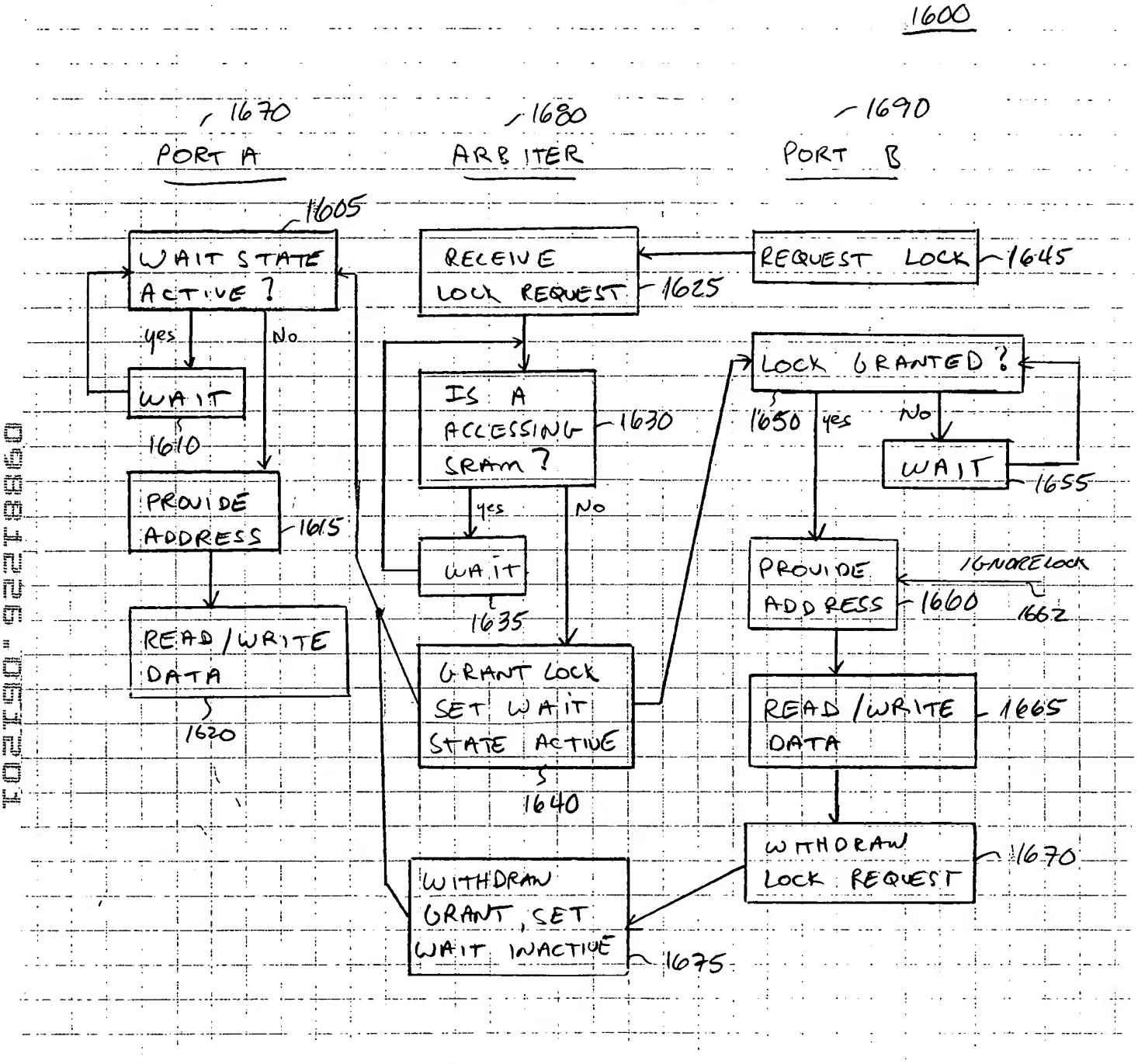


FIGURE 16

1700

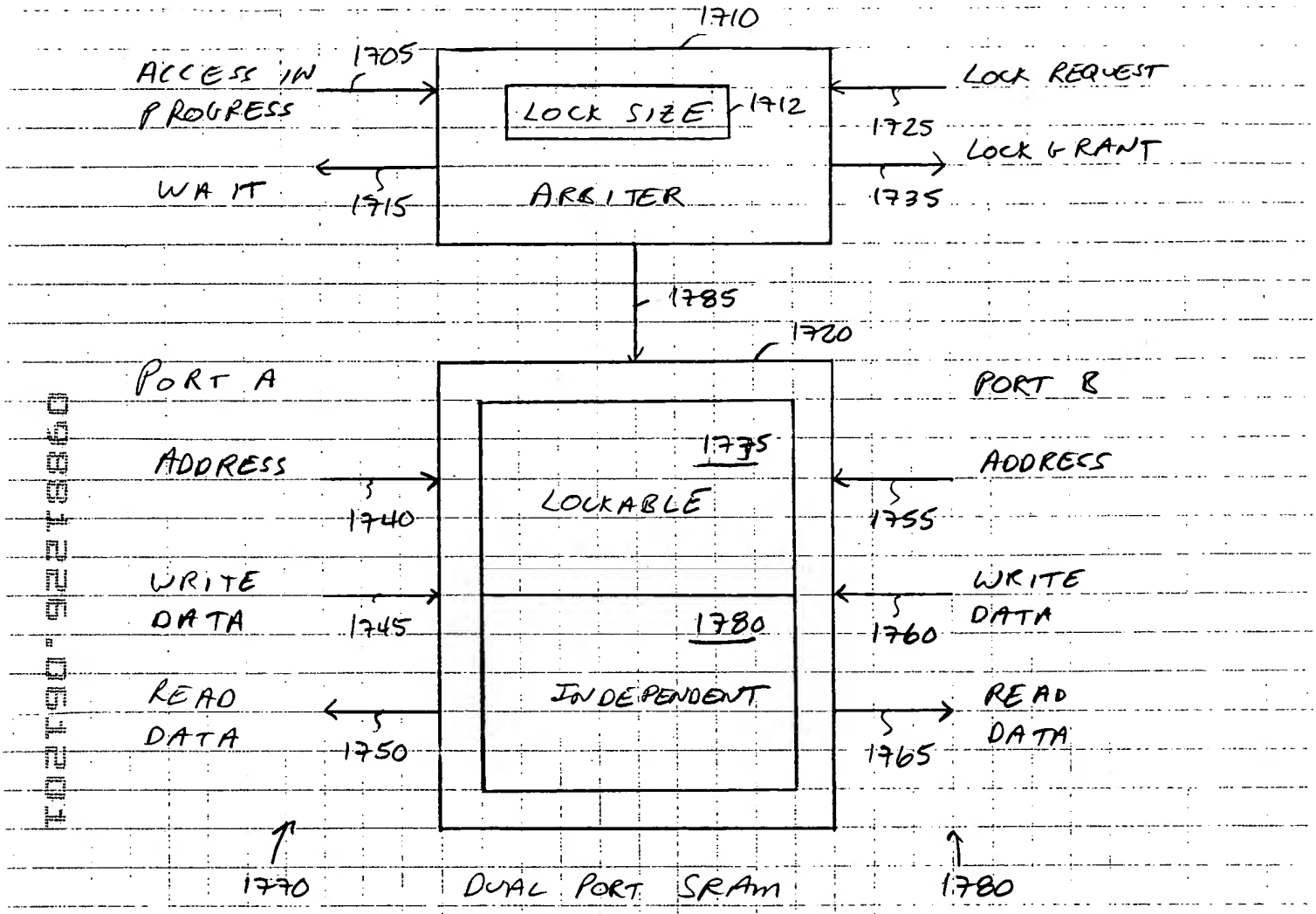


FIGURE 17

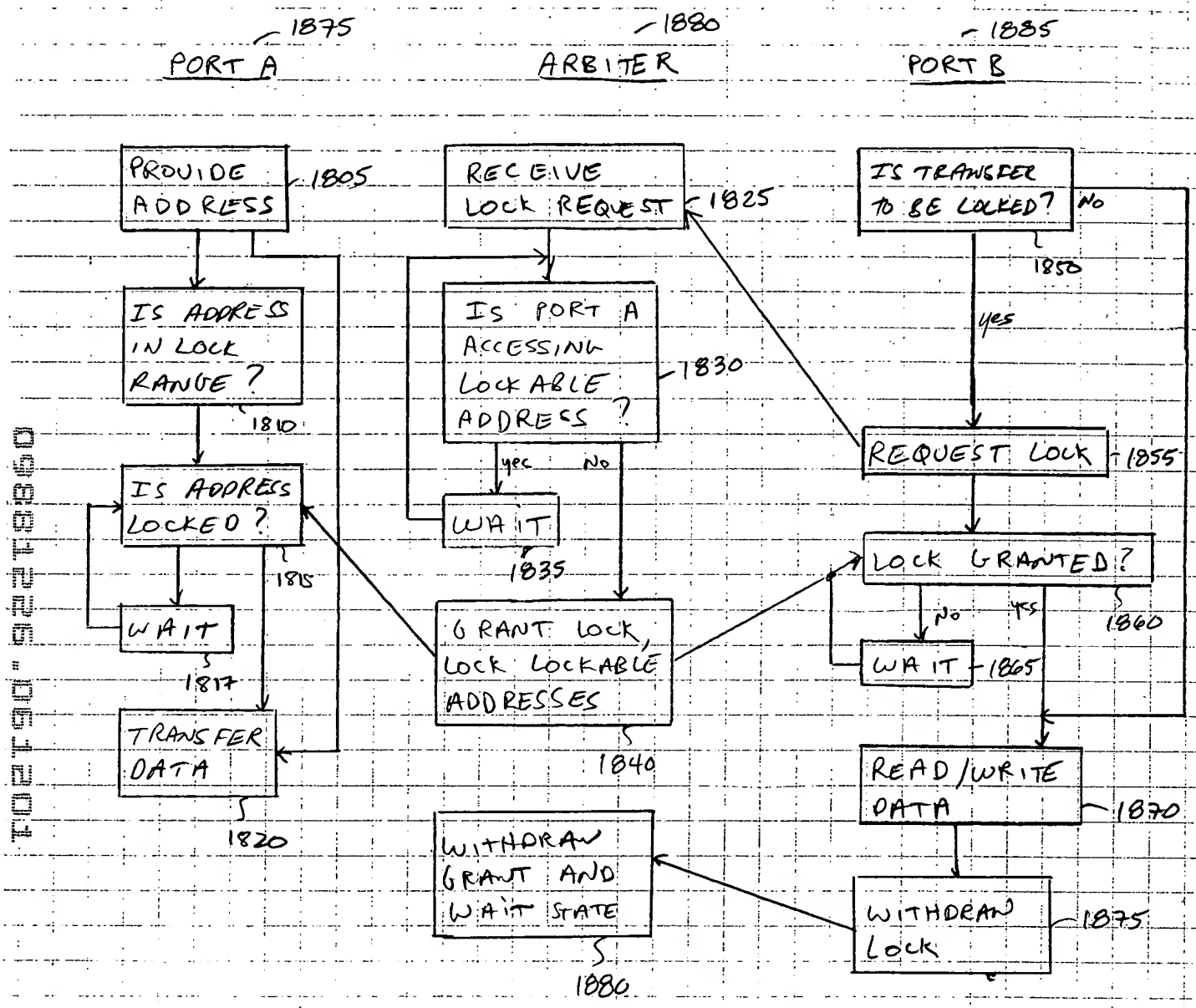

1800
1875
PORT A
1880
ARBITER
1885
PORT B
PROVIDE ADDRESS
1805
RECEIVE LOCK REQUEST
1825
IS TRANSFER TO BE LOCKED?
No
1850
yes
IS ADDRESS IN LOCK RANGE?
1810
IS PORT A ACCESSING LOCKABLE ADDRESS?
1830
REQUEST LOCK
1855
IS ADDRESS LOCKED?
1815
yes
No
WAIT
1835
LOCK GRANTED?
1860
No
yes
WAIT
1817
GRANT LOCK, LOCK LOCKABLE ADDRESSES
1840
WAIT
1865
TRANSFER DATA
1820
READ/WRITE DATA
1870
WITHDRAW GRANT AND WAIT STATE
1880
WITHDRAW LOCK
1875

FIGURE 18

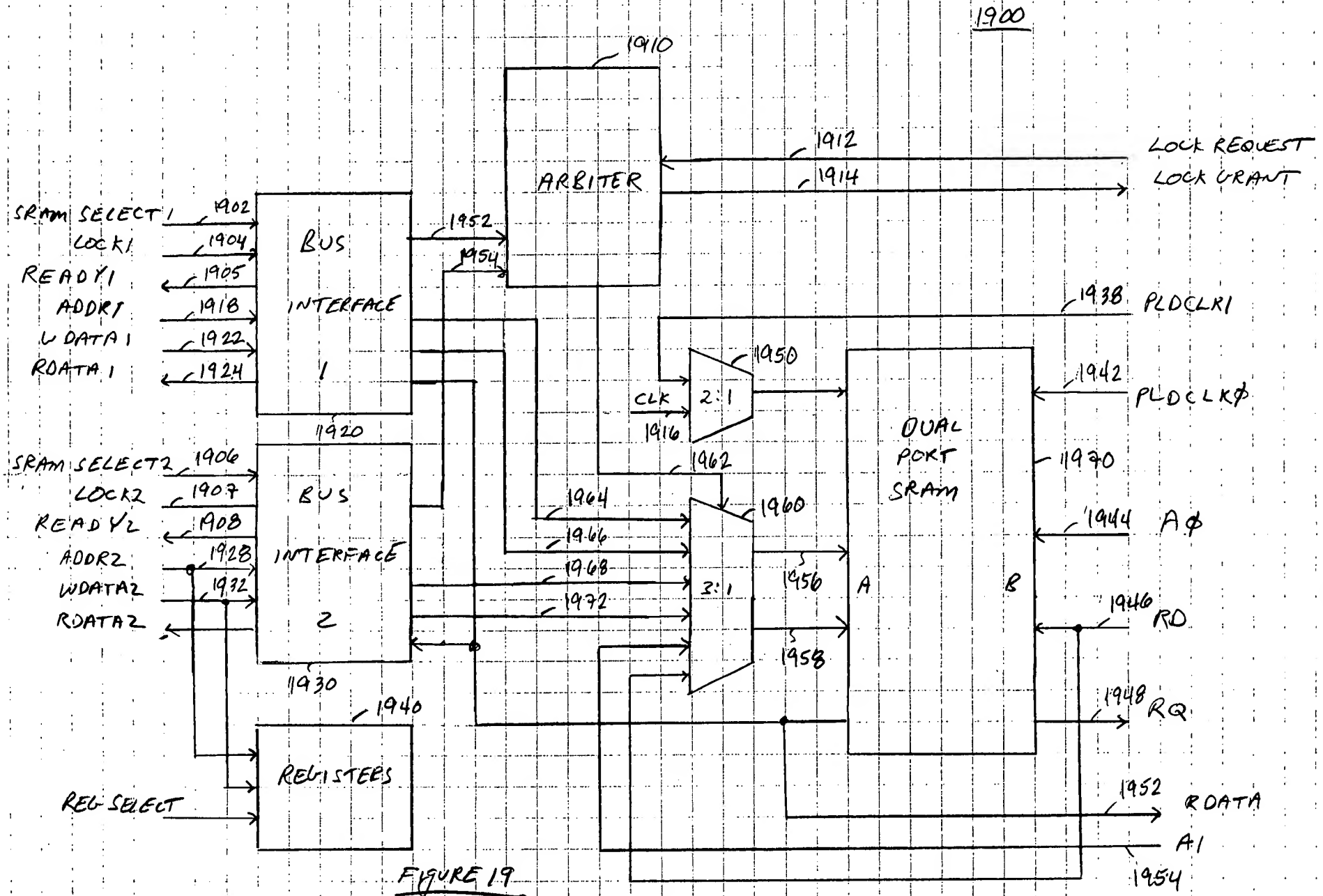


FIGURE 19

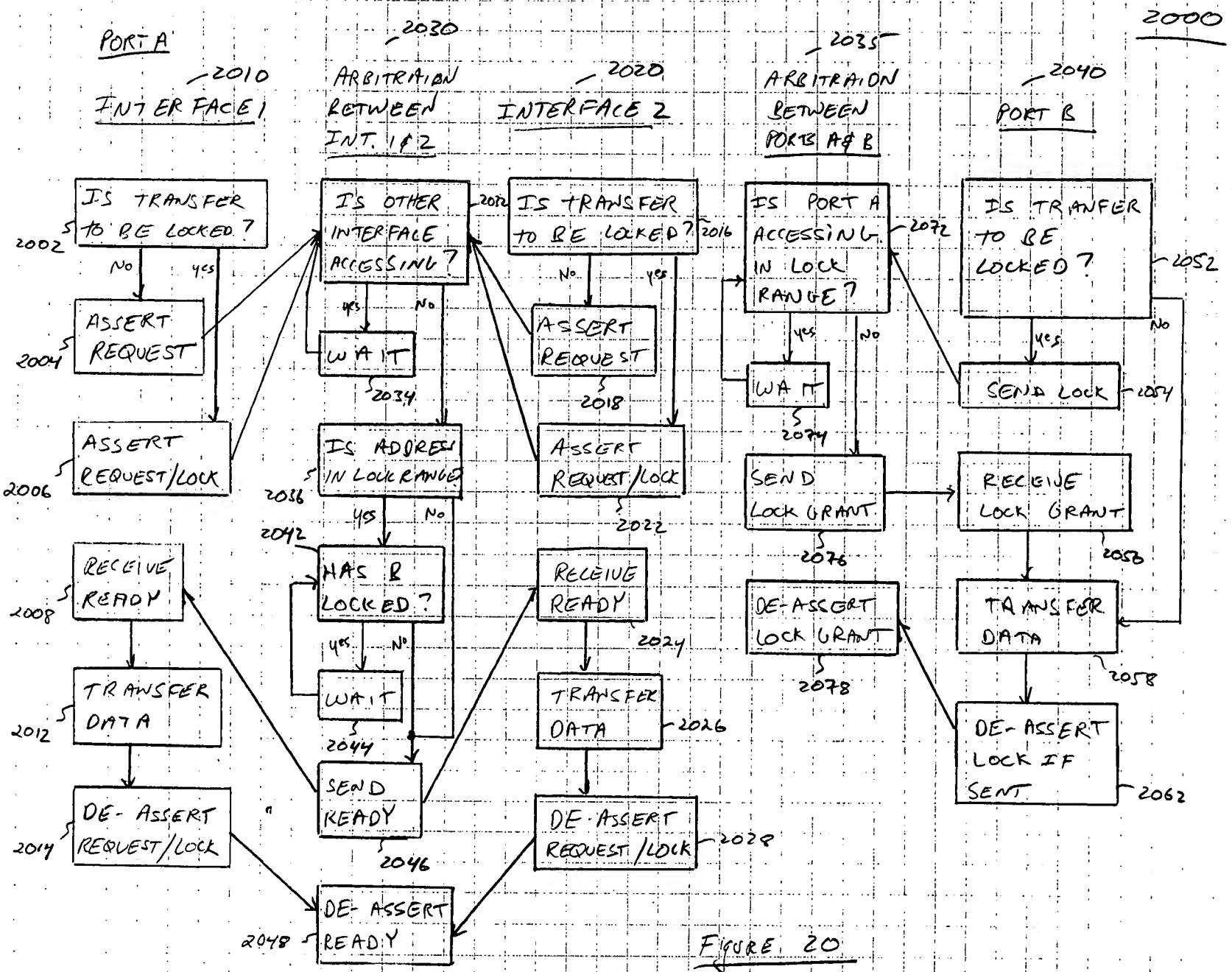


FIGURE 20

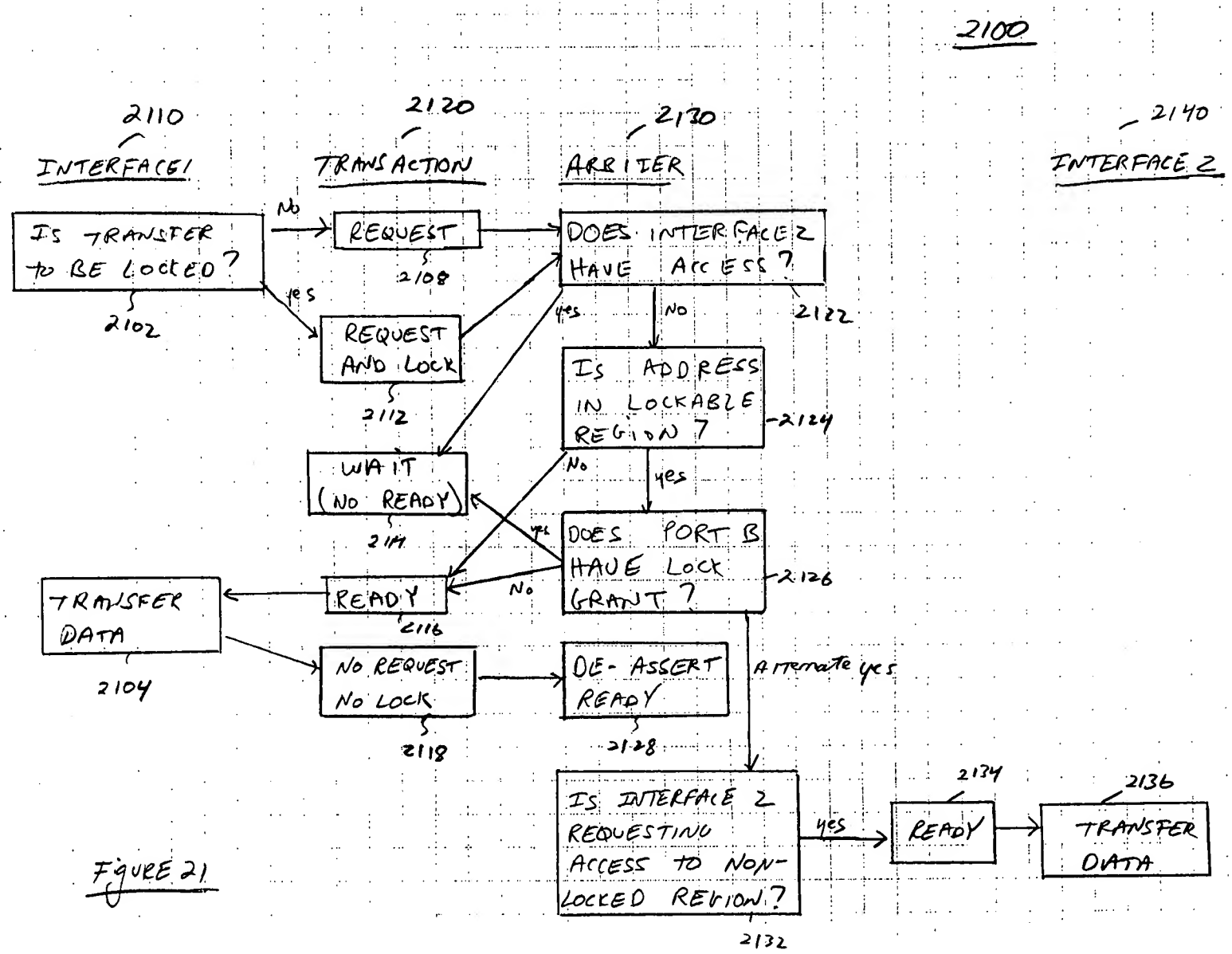


Figure 21

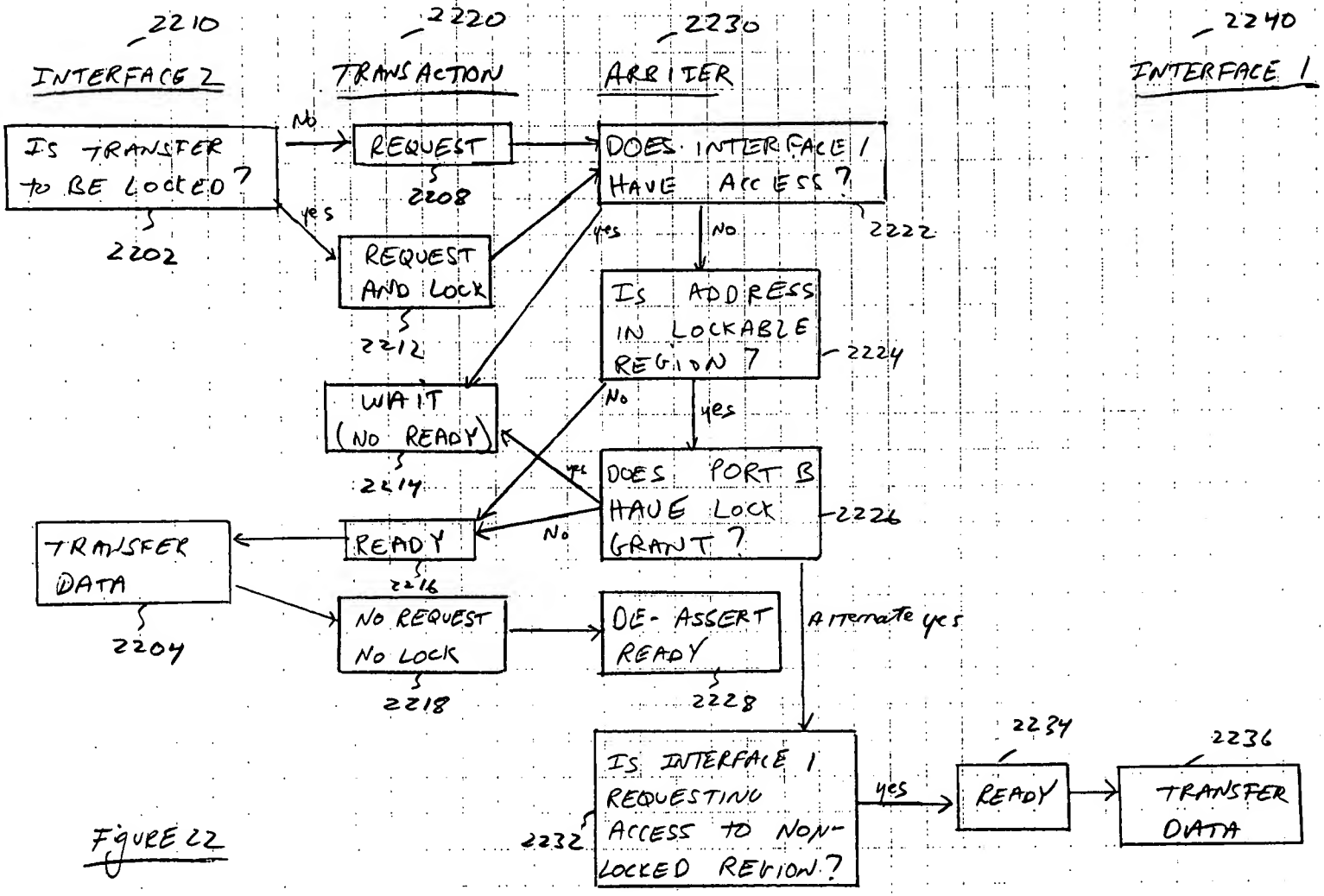

2210
INTERFACE 2
2220
TRANSACTION
2230
ARBITER
2240
INTERFACE 1
IS TRANSFER TO BE LOCKED?
2202
No
yes
REQUEST
2208
REQUEST AND LOCK
2212
DOES INTERFACE 1 HAVE ACCESS?
2222
yes
No
IS ADDRESS IN LOCKABLE REGION?
2224
No
yes
WAIT (NO READY)
2214
DOES PORT B HAVE LOCK GRANT?
2226
yes
No
READY
2216
TRANSFER DATA
2204
NO REQUEST NO LOCK
2218
DE-ASSERT READY
2228
Alternate yes
IS INTERFACE 1 REQUESTING ACCESS TO NON-LOCKED REGION?
2232
yes
2234
READY
2236
TRANSFER DATA

Figure 22

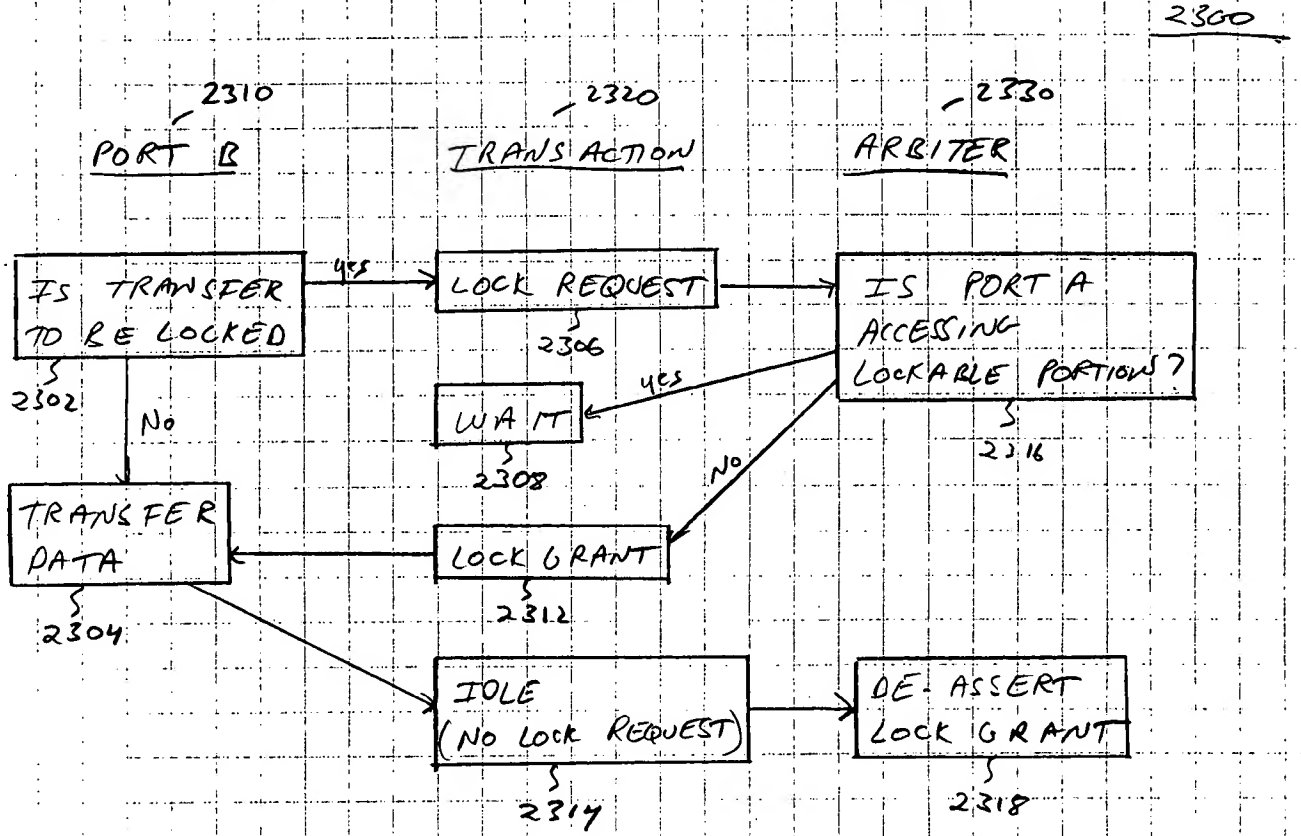


FIGURE 23

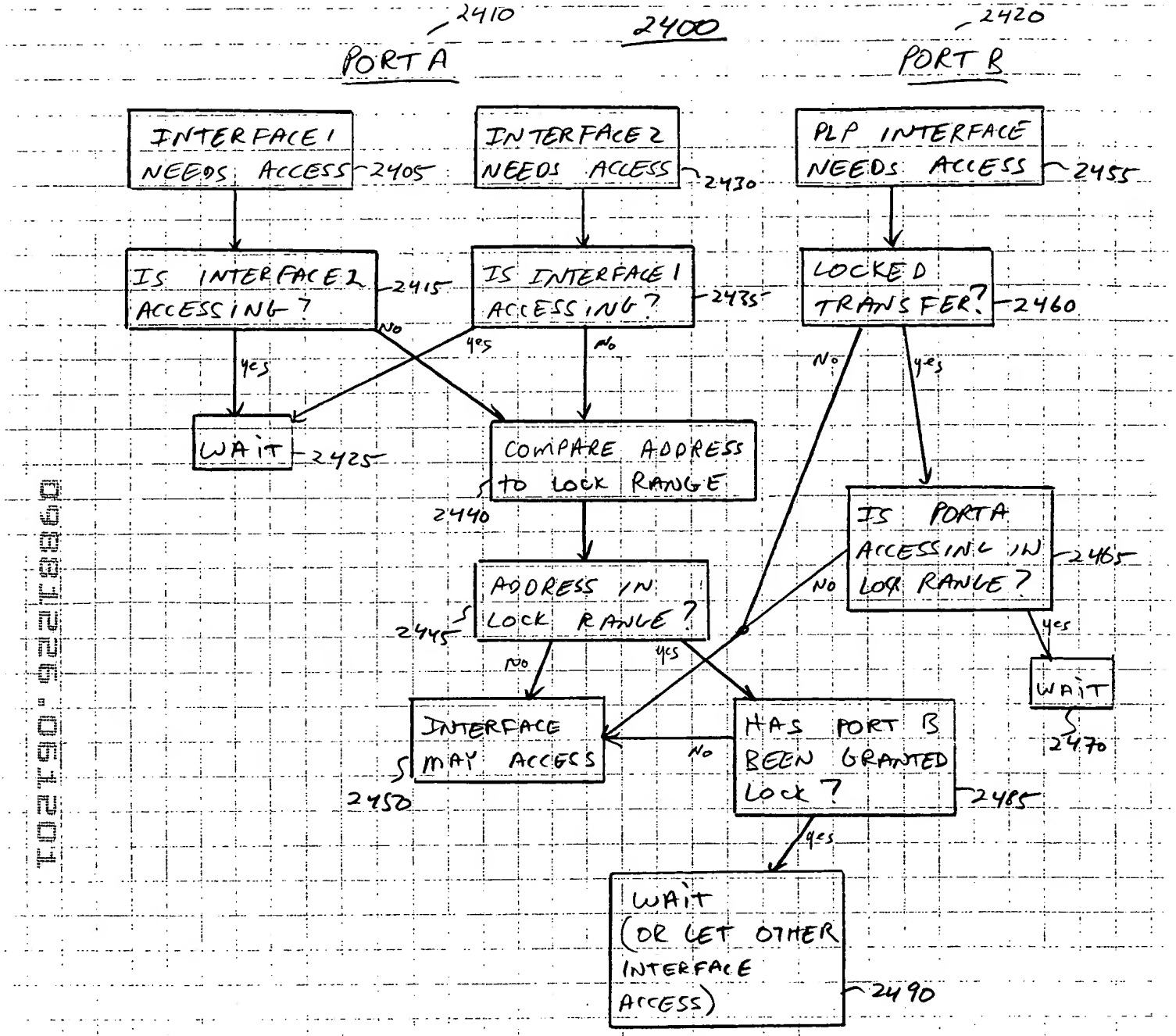

2400
2410
PORT A
2420
PORT B
INTERFACE 1 NEEDS ACCESS
2405
INTERFACE 2 NEEDS ACCESS
2430
PLP INTERFACE NEEDS ACCESS
2455
IS INTERFACE 2 ACCESSING?
2415
IS INTERFACE 1 ACCESSING?
2435
LOCKED TRANSFER?
2460
No
yes
yes
No
No
yes
WAIT
2425
COMPARE ADDRESS TO LOCK RANGE
2440
IS PORT A ACCESSING IN LOCK RANGE?
2465
No
yes
ADDRESS IN LOCK RANGE?
2445
No
yes
WAIT
2470
INTERFACE MAY ACCESS
2450
No
HAS PORT B BEEN GRANTED LOCK?
2485
yes
WAIT (OR LET OTHER INTERFACE ACCESS)
2490

FIGURE 24

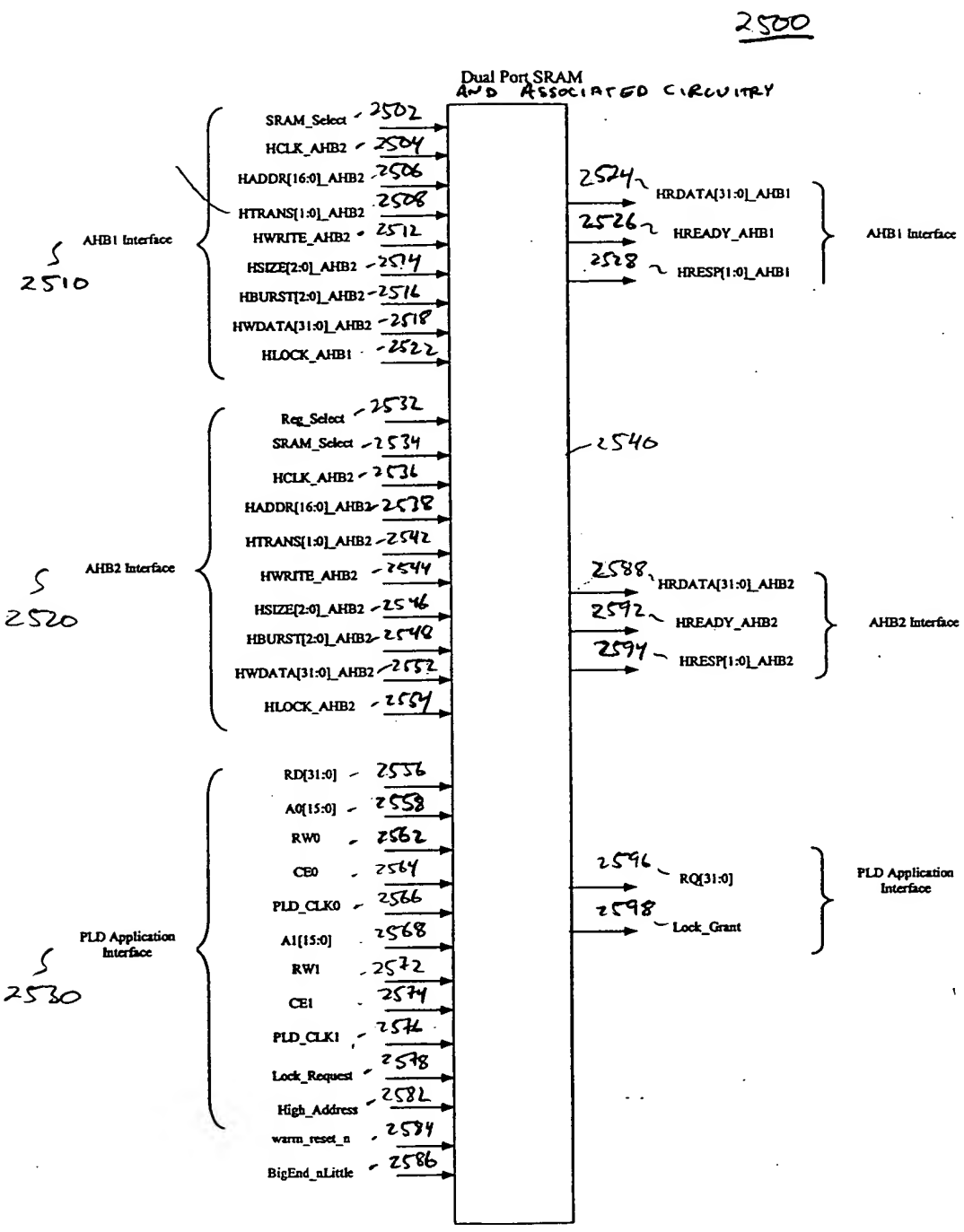


Figure 25